System:

ABSYS - Absolute Encoders

Based on the AMOSIN® – Inductive Measuring Principle

Types:

WMIA/WMKA Absolute Angular Encoder

LMIA/LMKA Absolute Linear Encoder

(for additional details, refer to www.amo-gmbh.com)

Implementation of serial interface in ABSYS encoders:

BiSS/C®

Note:

Chapter "1. Standard Encoder Profile" applies to all ABSYS Encoders

Chapters "2. Register Definition" and "3. Register Access" applies only to Encoders with BiSS-C Slave Revision 0x02 – See Chapter 2

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Document History:

Revision	Date	Author	Notes:
06	03.11.2011	Paul Tutzu	Description for Error and Warning bits
07	08.02.2014	Paul Tutzu	Register Access
08.02	01.04.2014	Paul Tutzu	Bank Access – BiSS/C Specification
08.03	18.09.2014	Paul Tutzu	BP3 Version 0x02 Addded

	Name		Name		Status
Author	Paul Tutzu	Update	Paul Tutzu	SP-EW InterfaceDescription_BiSSC_rev08.03.doc	**Released**
Date	12.10.2010	Date	18.09.2014		

Table of Contents:

1 Standard Encoder Profile – 32bits

The Standard Encoder Profile is used for grouping the linear and rotary encoder in accordance with the BiSS/C bidirectional protocol. For more information please read the document: "*BiSS C Protocol Description* from www.biss-interface.com.

The following data parameters must be used for configuring the BiSS/C master:

Protocol Type	Fully compatible with bidirectional and unidirectional[1] BiSS/C			
Data transfer and type	SCDS (Single Cycle Data Sensor)			
Bit Count	Position	notError	notWarning	Total
	32	1	1	34
Processing time	Minimum Acknowledge (Ack) signal length = 1 x Clock Frequency (MA) - No additional processing time is required[2]			
Data alignment	Right-aligned			
Error/Warning	Active on Low (0)			
CRC polynomial	$X^6 + X^1 + X^0$; or 0x43 – CRC bit length 6bits; inverted [3]			
CRC start value	"0"			
BiSS/C Timeout	Default – No special requirements			
Clock Frequency (MA)	max. 2.5 MHz [4]			
Power-on Delay[5]	1.8 sec			

Table.1 ABSYS Encoder – BiSS/C Configuration

[1] Register access is possible only when ABSYS Encoders are used with a BiSS/C master that supports bidirectional communication

[2] If a slave requires additional processing time before outputting its sensor data, it can request this by delaying the start bit (Ack – Acknowledge signal length several Clock Frequency). This does not apply to ABSYS encoders. ABSYS encoders do not require additional processing time; a new sensor data set is available in less than one SCD.

[3] See document "*BiSS Interface Application Note #3*" from www.biss-interface.com for more details about the CRC

[4] Clock Frequency is subject to further development. Please contact AMO for higher frequencies

[5] Power-on Delay: Required time between Power-On and valid encoder response

BiSS/C frame structure for ABSYS Encoders is presented in Figure 1.

Figure 1. BiSS/C frame structure in ABSYS Encoders

- **The Position field** (32 bits) contains the absolute position of the ABSYS encoders.

Example:

- **Angle Measuring Encoder -** WMKA-2x101.xxN-05120x,x-xx (see Brochure): The Position field (31:0) for this encoder with 512 pitches[1] per revolution, a pitch of 1000µm and 1024 increments/pitch can take values from 0x00000000 up to 0x0007FFFF; i.e. the Absolute Position is represented by 9 bits (512 pitches/revolution) plus 10 bits (1024 increments inside of one pitch). The resolution in arc length is 1000µm/1024 = 0.976..µm.

- **Length Measuring Encoder** – LMKA-x1101.xxx-x,x-xx: The Position field (31:0) for this encoder with a pitch of 1000µm and 1000 increments/pitch (1µm encoder resolution) can take values from 0x00000000[2] up to 0x0007CFFF when using a 512mm length measuring scale. (512 pitches x 1000 inc/pitch = 512,000 = 0x7D000 increments). The value of one LSB represents the resolution of the encoder.

- When an incorrect absolute position is read by the ABSYS encoder or the synchronization between incremental and absolute track is lost the **Error bit** is set to "0" (Error active). The error may occur after Power-On or during normal operation.
  - If the error occurs after Power-On the error remains latch
  - If the error occurs during normal operation and the synchronization is regain the error bit will be set back to "1" – No Error

- **Warning bit** is not used. Warning is always inactive and it is set to "1".

[1] Pitch = physical period of the measuring scale (or encoder disk for rotary encoders)
[2] Start position is not necessary to be 0. Length measuring scales may have a start position offset

2 Register definition

ABSYS Encoders allow access to internal registers, providing information used for unit identification and the Electronic Data Sheet (EDS). A comprehensive description of how registers can be access by a BiSS-C Master (e.g. Motion Controller) can be to be found in the *BiSS C Protocol Description" (Chapter "Control Communication")* - www.biss-interface.com

Registers address and function may change in the future. The actual revision of the BiSS-C Slave implemented in encoder is defined by the register: Revision (Address 0x7D). Chapters 1 and 2 apply only to Revision (Addr. 0x7D) = 0x02.

2.1 Register List

Address	Data Type	RW	Description	Default	Note
Bank #0-#127					
0x00 – 0x3F		x	Configuration Data	x	C.2.2
Bank #128 BiSS/C Electronic Data Sheet (EDS) – Common Part 1/4					
0x00 – 0x3F	U8	R	EDS Common Part	-	C.2.2
Bank #129 BiSS/C Electronic Data Sheet (EDS) – BP3 Part 2/4					
0x00 – 0x3F	U8	R	EDS Encoder Standard Profile BP3	-	C.2.2
Bank #130 BiSS/C Electronic Data Sheet (EDS) – Reserved 3/4					
0x00 – 0x3F	U8	x	EDS - Reserved	0x00	C.2.2
Bank #131 BiSS/C Electronic Data Sheet (EDS) – Reserved 4/4					
0x00 – 0x3F	U8	x	EDS - Reserved	0x00	C.2.2
Bank #132 User Data – OEM 1/4					
0x00 – 0x3F	U8	R/W	User/OEM Data	0x00	C.2.2
Reserved (Future Release - Bank #133 User Data – OEM 2/4)					
0x00 – 0x3F	U8	x	Reserved	0x00	C.2.2
Reserved (Future Release - Bank #134 User Data – OEM 3/4)					
0x00 – 0x3F	U8	x	Reserved	0x00	C.2.2
Reserved (Future Release - Bank #135 User Data – OEM 4/4)					
0x00 – 0x3F	U8	x	Reserved	0x00	C.2.2
0x40	U8	R/W	**Bank Selection**	0x80	C.2.2
0x41	U8	R/W	**EDS-Bank**	0x80	C.2.2
0x42-0x43	U16	R	**Profile ID**	0x6320	C.2.2
0x44-0x47	U32	R	**Serial Number**	-	C.2.5
0x48-0x4B		R	Reserved	0x00	
0x4C	U8	R/W	**Offset Value** (MSB) Bits: 31 ÷ 24	0x00	C.2.3
0x4D	U8	R/W	**Offset Value** Bits: 23 ÷ 16	0x00	C.2.3
0x4E	U8	R/W	**Offset Value** Bits: 15 ÷ 8	0x00	C.2.3
0x4F	U8	R/W	**Offset Value** (LSB) Bits: 7 ÷ 0	0x00	C.2.3
0x50-0x5F		R	Reserved	0x00	
0x60	U8	R/W	**Command Register**	0x00	C.2.3

Address	Data Type	RW	Description	Default	Note
0x61-62	U8	R	Reserved	-	
0x63	U8	R	**Position Data ST** (MSB) Bits: 31 ÷ 24	-	C.2.9
0x64	U8	R	**Position Data ST** Bits: 23 ÷ 16	-	C.2.9
0x65	U8	R	**Position Data ST** Bits: 15 ÷ 8	0x00	C.2.9
0x66	U8	R	**Position Data ST** (LSB) Bits: 7 ÷ 0		C.2.9
0x67-0x69			Reserved		
0x6A	U8	R/W	**Preset Mode**	0x00	C.2.3
0x6B	U8	R	**Error Status Register**	0x03	C.2.9
0x6C	U8	R	**Flash Status Register**	0x01	C.2.4
0x6D	U8	R	**Flash Error Register**	0xA5	C.2.4
0x6E	U8	R/W	**Flash Control Register**	0x80	C.2.4
0x6F-0x77		R	Reserved	-	
0x78-0x7C	U40	R	Device ID 1/2	0x00	
0x7D	U8	R	**Device ID 2/2 (Revision)**	0x02	
0x7E	ASCII	R	**Manufacturer ID – Char 1**	0x41 ("A")	A
0x7F	ASCII	R	**Manufacturer ID – Char 2**	0x6D ("m")	m

* Data saved as Big Endian (Most Significant Byte in lower address)

2.2 Bank Selection and EDS

Registers with addresses in range from 0x00 to 0x3F are organized in banks.

Address (0x40)	Bank	Description
0x00 – 0x7F	0-127	Device Configuration, no User Access
0x80	128	**Electronic Data Sheet – Common Part, Part 1/4**
0x81	129	**Electronic Data Sheet – Standard Profile BP3, Part 2/4**
0x82-0x83	130-131	Electronic Data Sheet – ***Reserved***, Part 3/4, 4/4
0x84	132	**User/OEM – Free to Write or/and Read**
0x85-0x87	134-135	Reserved – (Future Release - User/OEM)
0x88-0xFE	136-254	Reserved
0xFF	255	Not allowed

Bank selection is done using the Register 0x40. This register can be written or read but its value is not saved in non-volatile memory. After every Power-On/Reset the value of Bank Select register (address 0x40) will be 0x80 and Bank 128 is the active Bank.

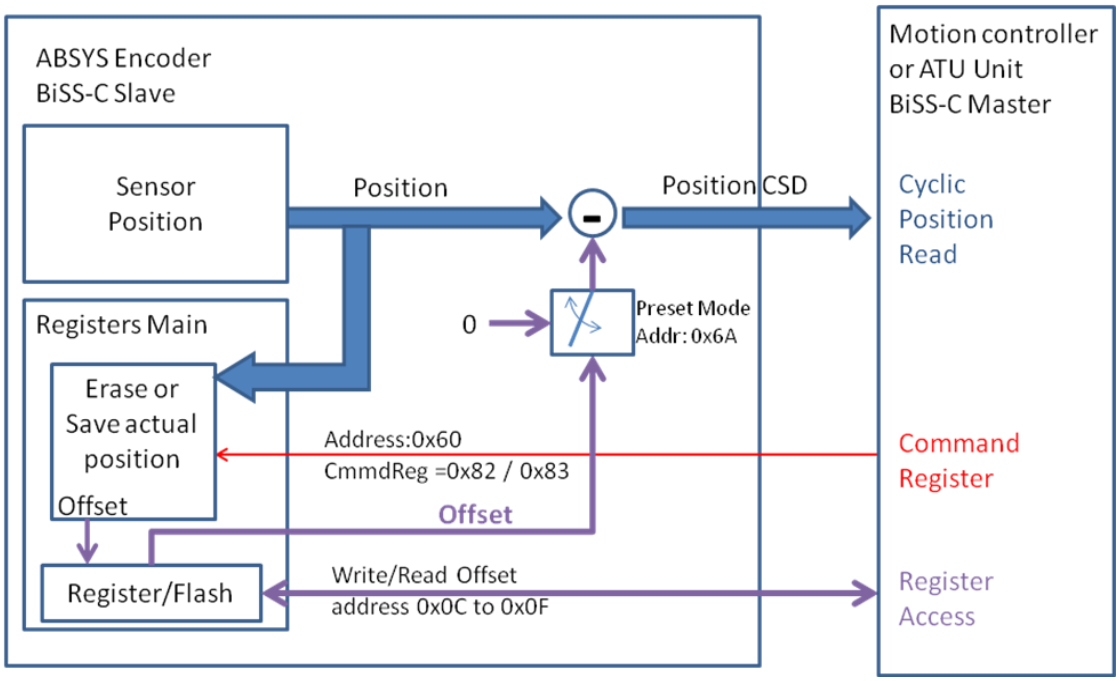
EDS Bank: Electronic Data Sheet – Common Part - Bank. Default value is 0x80. EDS Standard Profile banks and User/OEM Data banks addresses are saved in EDS Common Part.

Profile ID: The encoder profile used for AMO Encoders is ***BP3: Standard Encoder Profile.*** Default value for the Profile ID is:

Address	Value	Description
0x42	0x63	BP3, Version 1, CRC remaining to the data
0x43	0x20	Data length = 32 bits

2.3 Offset/Preset Function

Linear and rotary absolute encoders offer the possibility to use an offset value which will preset the Position provided by the Absolute Encoder. Offset value is normally used for presetting the commutation angle of the drive unit.



The maximum length of the offset is 32 bits. The offset values can be found at address:

No.	Address	Offset	Default value (Manufacturer)
1	0x4C	Offset 4 (31 down to 24)	0x00
2	0x4D	Offset 3 (23 down to 16)	0x00
3	0x4E	Offset 2 (15 down to 8)	0x00
4	0x4F	Offset 1 (7 down to 0)	0x00

Offset values can be updated:

1. By writing new values at address from above, using the standard BiSS-C Register Access.
2. By using the Command Register from address 0x60:

Command Register (0x60)	Description
0x00	Idle mode, module waits for a command (Standard Value)
0x02	Write the actual position to Offset (0x0C to 0x0F)
0x03	Reset (set to x"00000000") the actual Offset Values
0x06	Reset Encoder Errors

The Preset Mode (0x6A) can configure Position (sent during Cyclic Senor Data transfer):

Preset Mode (0x6A)	Description
0x00	Position CSD = Actual Position – Offset
0x01	Position CSD = Actual Position

- **Position displayed for Linear Encoders:**

POSITION_WITH_OFFSET = POSITION_ABSOLUTE – OFFSET

Where
- Linear Encoder: See parameter at Chapter 2.8.3
- POSITION_WITH_OFFSET – signed two's complement on 32 bits
- OFFSET – value saved in 0x4C – 0x4F

- **Position displayed for Rotary Encoders:**

POSITION_WITH_OFFSET = (POSITION_ABSOLUTE – OFFSET) ***MODULO*** PULSES_PER_REV

Where
- Rotary Encoder: See parameter at Chapter 2.8.3
- POSITION_WITH_OFFSET – unsigned on 32 bits
- OFFSET – value saved in 0x4C – 0x4F
- PULSES_PER_REV – pulses per revolution. See parameter Chapter 2.8.4

2.4 Flash Registers

All the Non-Volatile registers from the ABSYS Encoders are stored in a Flash Memory. For a better overview and control on the data transfer between registers and Flash memory the following Status/Control Registers are used:

Flash Status Reg. (0x6C) Read Only	Description
0x00	Initialization during encoder reset
0x01	Idle – Required state before and after a Write Command.
0x??	States during data processing

Flash Error Register (0x6D) Read only	Description
0xA5	No Error
0x84	Error - Flash not recognized
0x87	Error during Sector Erase
0x88	Error during Page Program
0x??	Not supported errors

Before starting a new Write Command it is required to check if the Flash Status Register (0x6C) is Idle - 0x01 and the Flash Error Register (0x6D) is No Error - 0xA5. Typical time needed for a Write command is around 2 sec.

Flash Error Register (0x6E) Read/Write	Description
0x00	Write control in flash is done automatically after a register value was updated. Not recommended for bulk data transfer.
0x80	Manual write control activated. The values are updated first in volatile register. 0x82 is required to transfer the data into Flash
0x82	Manual command to write all the values from registers to Flash. If the operation was completely successfully the values sets back to 0x80. Check also the Flash Error and Status registers. (0x6C and 0x6E)

2.5 Serial Number

Serial number is stored in 4 Bytes in Binary format. The value is saved as Big Endian, i.e. with the highest-value byte at the lowest-value address. Example:

SN Decimal	SN(MSB) 0x44	SN 0x45	SN 0x46	SN(LSB) 0x47
H1412345	0x00158CF9			
	0xF9	0x8C	0x15	0x00

2.6 Encoder Position and Error

Encoder position sent during the Cyclic Sensor Data (CSD) is also available in Registers from address: 0x63 (MSB) up to 0x66 (LSB).

Encoder error and warning send during the CDS are also available in Registers at address 0x6B. The difference is that in the register all the encoder errors or warnings are latched. The errors/warning can be reset sending the command 0x06 from register Command Register – Address 0x60. (See Chapter 2.2)

Error Status Register (Addr. 0x6B)	Description
Bit 0	Encoder/Sensor warning
Bit 1	Encoder/Sensor error
Bit 2 - 7	Set to 0. To be defined.

2.7 EDS Common Part

Address	Data Type	RW	Description	Default	Note
0x00	U8	R	EDS Version (continuous number)	0x01	2.7.1
0x01	U8 (Banks)	R	EDS length (bank count completely)	0x02	2.7.2
0x02	U8	R	Bank address USER start	0x84	2.7.3
0x03	U8	R	Bank address USER end	0x84	2.7.3
0x04-0x0F	U8	R	***To be defined***	0x00	
0x10	U8	R	Number of data channel in this device	0x01	
0x11	U8	R	Area of validity for this EDS	0x01	
0x12	U8	R	Memory location for this EDS	0x80	
0x13			Reserved		
0x14	U8	R	Bank address for content description data Ch.1	0x81	2.7.4
0x15	U8 (bit)	R	Data length data channel 1	0x20	
0x16	U8 (bit)	R	Data format data channel 1	0x00	
0x17	U8	R	CRC polynome (8:1) for data channel 1	0x21	
0x18-0x34	U8	R	***To be defined***	0x00	
0x35-0x3E			Reserved		
0x3F	U8	R	Checks sum		

2.7.1 EDS Version

Current Electronic Datasheet (EDS) Version.

2.7.2 EDS Length

Number of Banks for EDS. Default value is 2: one bank for Common Part and one bank for Standard Profile BP3.

2.7.3 Bank Address User

Start and End bank address for the User/OEM data.

2.7.4 Bank address for content description data Ch.1

Bank address for Standard Profile BP3.

* Data saved as Big Endian (Most Significant Byte in lower address)

2.8 EDS Standard Profile BP3 (Version BP_VER 0x01) – Obsolete!

Obsolete – Not for new design!

Address	Data Type	RW	Description	Default	Note
0x00	U8	R	Version (BP_VER)	**0x01**	
0x01	U8 (Banks)	R	Length of this profile (BP_LEN)	0x01	2.8.1
0x02	U8	R	Profile Identification Part 1/2 (Adr.0x42) (BP_ID)	0x63	2.8.2
0x03	U8	R	Profile Identification Part 2/2 (Adr.0x43) (BP_ID)	0x20	2.8.2
0x04	U8	R	Feedback bit 1 (error = 1, warning = 2) (FB1)	0x01	
0x05	U8	R	Feedback bit 2 (error = 1, warning = 2) (FB2)	0x02	
0x06	U8 (ms)	R	Maximum "power on delay" (PON_PDL)	0xFF	
0x07			Reserved	0x00	
0x08	U8	R	Encoder type (EN_TYP)		2.8.3
0x09	U8	R	Position Value (POS_NUM)	0x01	
0x0A	U8 (bit)	R	Data length MULTITURN (MT_LEN)	0x00	
0x0B	U8	R	Data format MULTITURN (MT_FMT)	0x00	
0x0C	U8 (bit)	R	Data length COARSE (CO_LEN)	0x00	
0x0D	U8	R	Data format COARSE (CO_FMT)	0x00	
0x0E	U8 (bit)	R	Data length FINE (FI_LEN)	0x20	
0x0F	U8	R	Data format FINE (FI_FMT)	0x00	
0x10-0x13	U32	R	Number of distinguishable periods (MT_CNT)	0x00000000	
0x14-0x17	U32 (nm/ppr)	R	Length of signal period (linear) (SIP_CNT) Number of signal periods per revolution(rotary)		2.8.4
0x18-0x1B	U32 (bit)	R	Resolution factor per signal period (SIP_RES)	0x00000001	2.8.4
0x1C-0x1F	U32	R	CRC polynome (31:1) (CPOLY)	0x00000021	
0x20-0x23	U32	R	CRC start value (CSTART)	0x00000000	
0x24-0x39	U8	R	***To be defined***	0x00	
0x3A-0x3E			Reserved	0x00	
0x3F	U8	R	Check sum		

2.8.1 Length of this profile (BP_LEN)

Number of Banks for this profile (BP3).

2.8.2 Profile Identification (BP_ID)

Profile Identification, BP3, 32 bits.

2.8.3 Encoder Type (EN_TYP)

Rotary Encoder 0x00, Linear Encoder 0x01.

2.8.4 Encoder Resolution

For linear encoder: SIP_CNT – Resolution in nm and SIP_RES = 0x01.
For rotary encoders: SIP_CNT = Pulses / revolution. SIP_RES = 0x01,

* Data saved as Big Endian (Most Significant Byte in lower address)

2.9 EDS Standard Profile BP3 (Version BP_VER 0x02)

Address	Data Type	RW	Description	Default	Note
0x00	U8	R	Version (BP_VER)	**0x02**	
0x01	U8 (Banks)	R	Length of this profile (BP_LEN)	0x01	2.9.1
0x02	U8	R	Profile Identification Part 1/2 (Adr.0x42) (BP_ID)	0x63	2.9.2
0x03	U8	R	Profile Identification Part 2/2 (Adr.0x43) (BP_ID)	0x20	2.9.2
0x04	U8	R	Feedback bit 1 (error = 1, warning = 2) (FB1)	0x01	
0x05	U8	R	Feedback bit 2 (error = 1, warning = 2) (FB2)	0x02	
0x06	U8 (ms)	R	Maximum "power on delay" (PON_PDL)	**0xFF**	2.9.5
0x07			Reserved	0x00	
0x08	U8	R	Encoder type (EN_TYP)		2.9.3
0x09	U8	R	Position Value (POS_NUM)	0x01	
0x0A	U8 (bit)	R	Data length MULTITURN (MT_LEN)	0x00	
0x0B	U8	R	Data format MULTITURN (MT_FMT)	0x00	
0x0C	U8 (bit)	R	Data length COARSE (CO_LEN)	0x00	
0x0D	U8	R	Data format COARSE (CO_FMT)	0x00	
0x0E	U8 (bit)	R	Data length FINE (FI_LEN)	0x20	
0x0F	U8	R	Data format FINE (FI_FMT)	0x00	
0x10-0x13	U32	R	Number of distinguishable periods (MT_CNT)	0x00000000	
0x14-0x17	U32 (nm/ppr)	R	Length of signal period (linear) (SIP_CNT) Number of signal periods per revolution(rotary)		2.9.4
0x18-0x1B	U32 (bit)	R	Resolution factor per signal period (SIP_RES)		2.9.4
0x1C-0x1F	U32	R	CRC polynome (31:1) (CPOLY)	0x00000021	
0x20-0x23	U32	R	CRC start value (CSTART)	0x00000000	
0x24-0x39	U8	R	***To be defined***	0x00	
0x3A-0x3E			Reserved	0x00	
0x3F	U8	R	Check sum		

2.9.1 Length of this profile (BP_LEN)

Number of Banks for this profile (BP3).

2.9.2 Profile Identification (BP_ID)

Profile Identification, BP3, 32 bits.

2.9.3 Encoder Type (EN_TYP)

Rotary Encoder 0x00, Linear Encoder 0x01.

2.9.4 Encoder Resolution

For linear encoder: SIP_CNT – Resolution in nm and SIP_RES = 0, 1, 2 …20.

For rotary encoders: SIP_CNT = Pulses / revolution. SIP_RES = 0, 1, 2 … 20.

Rotary Encoder:

Pulses / Revolution = SIP_CNT x 2^SIP_RES

Linear Encoder:

Resolution LSB [nm] = SIP_CNT [nm] / 2^SIP_RES

* Data saved as Big Endian (Most Significant Byte in lower address)

2.9.5 Maximum Power-on Delay

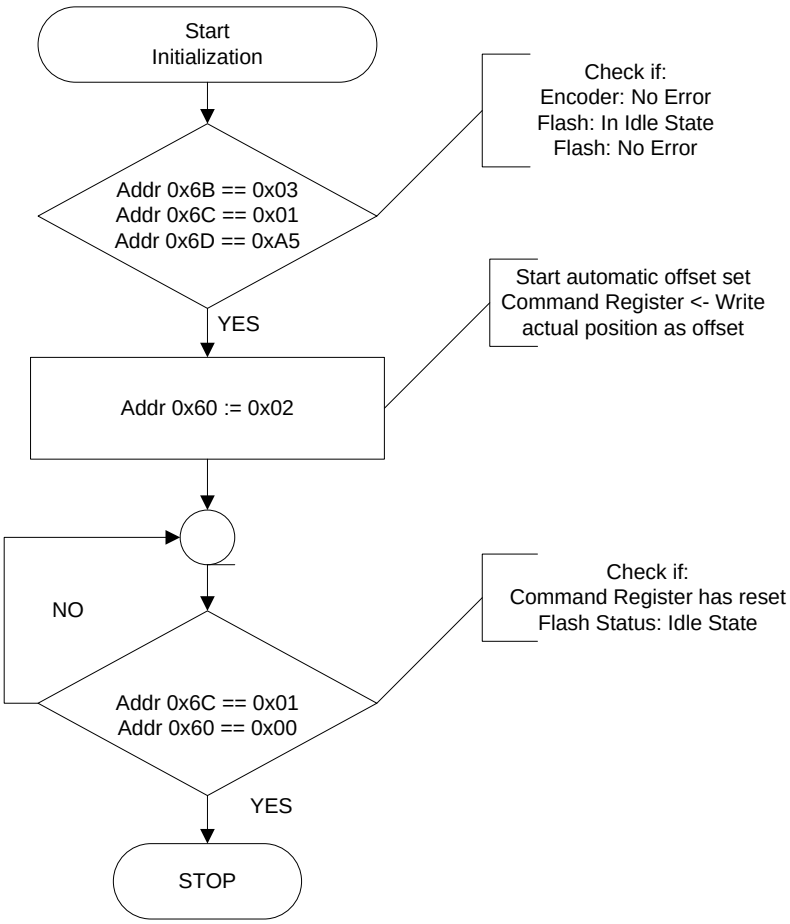
PON_PDL is defined as: Maximum "power on delay" until position data is available (BiSS Interface – BP3: Standard encoder profile. Revision A2, Page 6/14).
Maximum allowed value in the BP3 Profile is 254 ms.

!! AMO Absolute Encoders ABSYS requires 1.8 sec from Power On (Supply Voltage is stable) until the Encoder response to a position request with valid data !!

3 Register Access

3.1 Update offset value

The easiest way to update the offset value (Addr 0x0C up to 0x0F) is to use the Command Register (Addr 0x60). Writing 0x02 to this Register will update the offset value with the current position. Writing 0x03 will reset the offset to zero.
Offset can also be updated using the standard Write command to the 0x0C – 0x0F addresses.

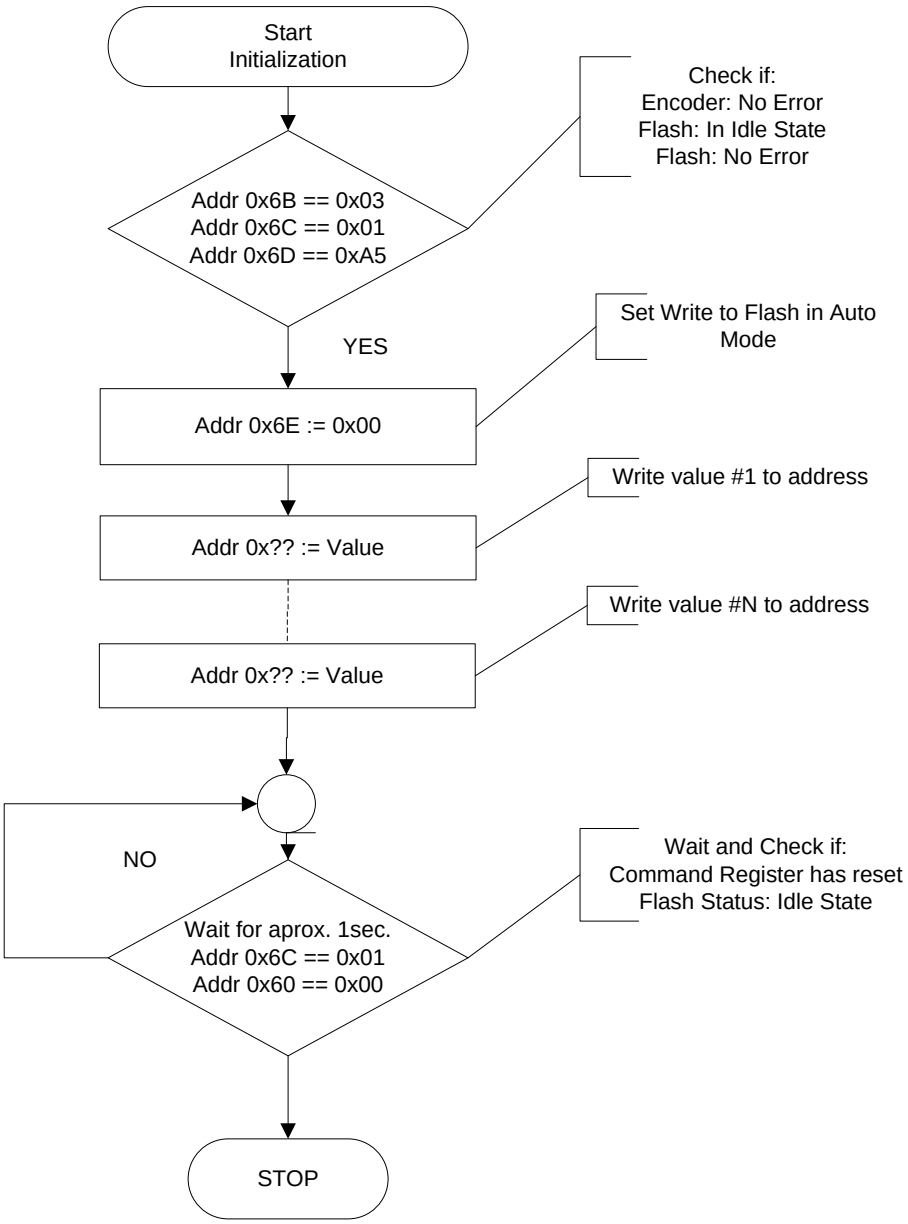


! For the Offset Update please pay attention to the value of: PRESET_MODE (0x6A) !

3.2 Write in Auto Mode

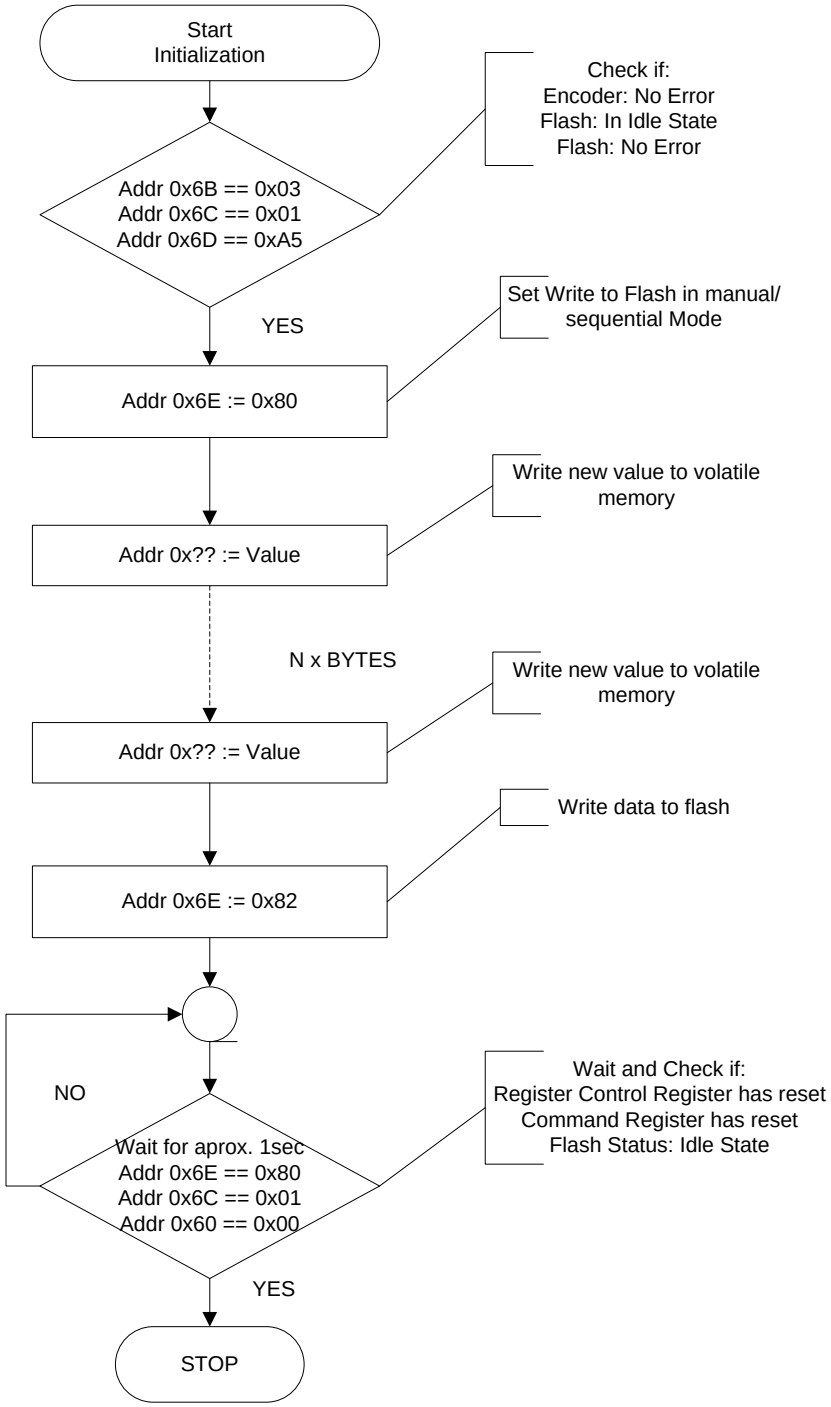
Auto Mode Write is active when the Flash Control Register (Addr: 0x6E) is set to **0x00**. After each write command from the BiSS-C Master the Encoder will write the received value to Flash Memory.
~~That is why, before sending another write command the master must check the Flash Status Register (Addr: 0x6C) and wait until the state is IDLE.~~
~~The main drawback of the Auto Mode Write is the required time. A Flash Write Cycle is around 3 sec. This means for N bytes the required time is N sec.~~

This applies to all address locations which are defined as W/R except the Command Register (Addr: 0x60).



3.3 Write in Manual Mode

Manual Mode Write is active when the Flash Control Register (Addr: 0x6E) is set to **0x80**. Manual Mode differs from the Auto Mode from the fact that the BiSS-C Master is the one who decides when to writes the values to FLASH. All the values are written first to a volatile memory and the Flash Control Register (0x6E) set to 0x82 initiate writing the values to FLASH. Time required for N bytes is only 1 sec. (This applies also to all R/W Registers except Command Register Addr 0x60).



4 Appendix

4.1 Non-Volatile Memory (Flash) Timing

Register are saved in an internal non-volatile memory (Flash). During the Write Register Command the BiSS-C Master must take caution and check and wait and wait until a write operation was successfully completed before starting another one. See Chapter 2.3 for the list with the registers for Flash Status, Error and Control.

A Write Command has two operations:

No.	Steps	Typical	Maximum
1st	Sector Erase	1.0 s	3 s
2nd	Page Program	1.4 ms	5 ms
Write Command Total		**1001.4 ms**	**3005 ms**

4.2 Flash Mapping

Address (0x40)	Bank	Flash Address
0x00 – 0x7F	0-127	n.a.
0x80	128	0x000-0x03F
0x81	129	0x080-0x0BF
0x82-0x83	130-131	n.a.
0x84	132	0x0BF-0x0FF
0x85-0x87	133-135	n.a.
0x88-0xFF	136-255	n.a.

5 Revision

Revision 8.03 - Chapter 1. Standard Encoder Profile: Power-on Delay added - Chapter 2.8 Obsolete - Chapter 2.9. Added – BP3 Profile Revision 0x02