



Specification

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Interface Description - SSI

Date

Rev.

15.01.2018

01.02

System: **ABSYS - Absolute Encoders**
Based on the AMOSIN® – Inductive Measuring Principle

Types: **WMIA** Absolute Angular Encoder

LMIA Absolute Linear Encoder

(for additional details, refer to www.amo-gmbh.com)

Implementation of output interface in ABSYS encoders:

SSI

Document History:

Revision	Date	Author	Notes:
01.00	25.11.2016	A.Pommer	Initial version
01.01	18.09.2017	A.Pommer	Order code corrected
01.02	15.01.2018	A.Pommer	Update/additional information Table 3

	Name		Name		Status
Author	A.Pommer	Update	A.Pommer	SP-EW InterfaceDescription_SSI_P6.rev01.02 .docx	released
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1. Power supply Specification

Supply voltage:	DC 3,6V to 14V
Power consumption (typ.):	300 mA@5,0V

Table 1

2. Turn on Time

Turn on time reading head:	≤ 2 s
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Table 2

3. Interface Protocol

3.1 General Description

The position value is transmitted synchronously to the clock signal of the control system starting with the most significant bit (MSB). When non-operational the clock as well as the data line is high. As soon as the clock signal of a clock sequence changes for the first time from high (H) to low (L), the parallel data will be stored in an internal shift register. This ensures that the data cannot change during the transmission of a position value. With the following rising edge transition of the clock signal, the transmission begins with the most significant bit (MSB). With each following rising edge transition of the clock signal, the next lower significant bit is set on the output of the data line. After the least significant bit was shifted out, the last rising edge transition of the clock signal switches the data line to low (transmission end).

> Description – Error bit:

The integrity of the absolute position is checked every 0.5mm. When an incorrect absolute position is read by the ABSYS encoder the **Error bit** is set to "1" (Error active). The error may occur after Power-On or during normal operation

> Description – Warning bit:

Warning bit is not used. Warning is always inactive and it is set to "0".

> End of transmission / pause time:

After the last falling edge of the clock signal, a retriggerable mono-flop determines with its internal delay time t_m , how long it will take until the encoder can be selected for the next transmission. With this, the minimal admissible break time between two successive clock sequences is determined.

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3.2 Timing

Clock frequency :	200 kHz – 1 MHz		
Monoflop time - t_m :	30 μ s		
Logic state during t_m :	Dataline – low (see diagram 1)		
Number of bits	Order Code	Number of bits - m:	Number of databits - N:
	WMKA2x10S <u>.18</u> LMKAxx10S <u>.18</u> ²⁾	28	25
	WMKA2x10S <u>.15</u> LMKAxx10S <u>.15</u>	31	28
	WMKA2x10S <u>.19</u> LMKAxx10S <u>.19</u> ¹⁾	33	30
Number of special bits:	3		
Type of special bits:	S0 ... parity [even]		
	S1 ... warning		
	S2 ... error		
Placement of special bits	placed after data bits (see diagram 1)		
Logic state of special bits	high active		

- Notes:
- 1) Scale length > 9200mm up to 32000mm
 - 2) **Used only in case of backwards compatibility. Not recommended for new designs. Please contact AMO if needed (max. coded length < 9200mm!)**

Table 3

Timing diagram:

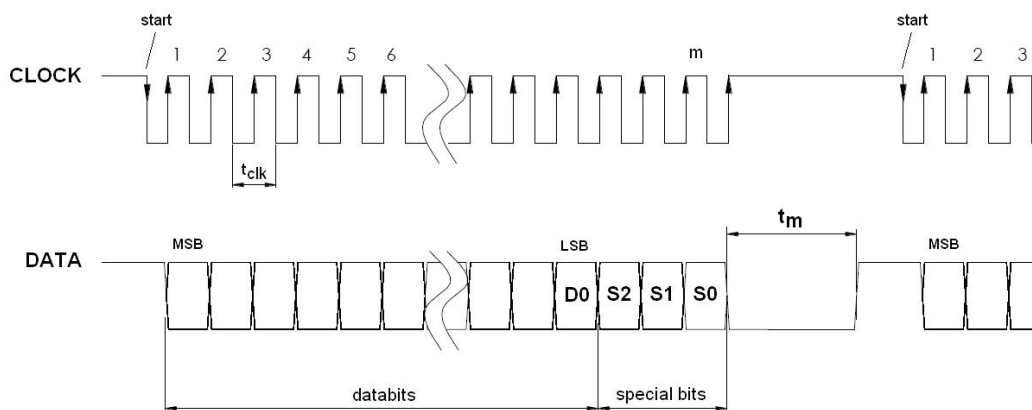


Diagram 1

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3.3 Coding of absolute value

Position data is coded binary (for details - see table 4). First data bit represents MSB.

3.3.1 Absolute encoder rotary – WMIA

Absolute rotary coding:

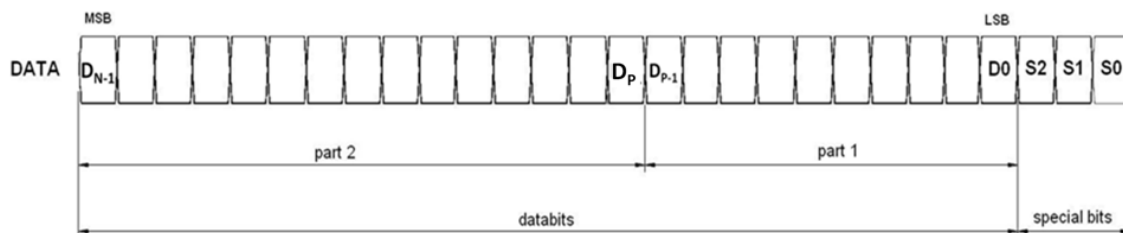


Diagram 2

Databits :																					
part 2:	$D_{N-1} \div D_p$ circumference in mm, binary coded																				
part 1:	$D_{p-1} \div D_0$ position inside one grating pitch ¹⁾																				
	<p>"P"-value depends on the Resolution in bit per grating pitch</p> <ul style="list-style-type: none"> When Resolution/Pitch is 10bit → P = 10 When Resolution/Pitch is 12bit → P = 12 																				
	<p>Example: WMKA2010S.1810..xx-20- 256-x,xx-xxxx-xx</p> <ul style="list-style-type: none"> Resolution in bit per grating pitch is 10 bits (N=25, P=10): <ul style="list-style-type: none"> Data bits – Part 1 (10bits): $D_9 \div D_0$ Data bits – Part 2 (15bits): $D_{24} \div D_{10}$ SSI Frame: 																				
	<table border="1"> <thead> <tr> <th colspan="2">Data Bits</th> <th colspan="3">Special Bits</th> </tr> <tr> <th>Part 2</th> <th>Part 1</th> <th>Er</th> <th>Wr</th> <th>Par</th> </tr> </thead> <tbody> <tr> <td>000000010110011</td> <td>1100010101</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>179 (179/255)</td> <td>789 (789/1023)</td> <td>No Error</td> <td>No Warning</td> <td>Parity OK</td> </tr> </tbody> </table>	Data Bits		Special Bits			Part 2	Part 1	Er	Wr	Par	000000010110011	1100010101	0	0	0	179 (179/255)	789 (789/1023)	No Error	No Warning	Parity OK
Data Bits		Special Bits																			
Part 2	Part 1	Er	Wr	Par																	
000000010110011	1100010101	0	0	0																	
179 (179/255)	789 (789/1023)	No Error	No Warning	Parity OK																	

Notes: ¹⁾ grating pitch = 1mm

Table 4

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3.3.1 Absolute encoder linear – LMIA

Absolute linear coding:

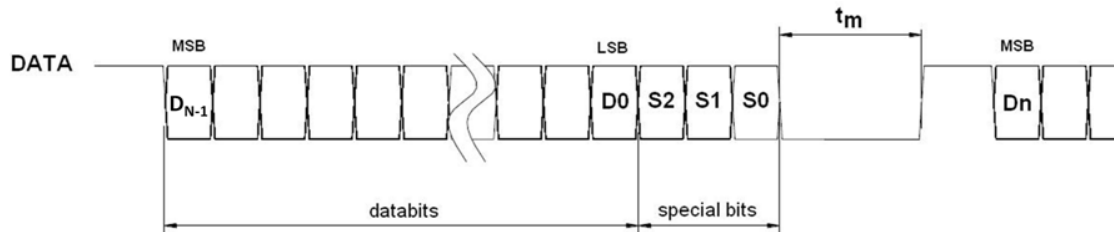


Diagram 3

Databits :	$D_{N-1} \div D_0$ <ul style="list-style-type: none"> 1 LSB represents the Encoder Resolution (e.g. 1μm) - binary coded. Data is right aligned. Unused MSBs are filled with '0'. 														
	<p>Example: LMKA2010S 1810..xx-20-xx x,xx-xxxx-xx</p> <ul style="list-style-type: none"> Resolution is 1μm Data bits width: 25 bits (N = 25) SSI Frame: <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th rowspan="2">Data Bits</th> <th colspan="3">Special Bits</th> </tr> <tr> <th>Er</th> <th>Wr</th> <th>Par</th> </tr> </thead> <tbody> <tr> <td>00000001011100111100010101</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Absolute position = 184'085 μm</td> <td>No Error</td> <td>No Warning</td> <td>Parity OK</td> </tr> </tbody> </table>	Data Bits	Special Bits			Er	Wr	Par	00000001011100111100010101	0	0	0	Absolute position = 184'085 μ m	No Error	No Warning
Data Bits	Special Bits														
	Er	Wr	Par												
00000001011100111100010101	0	0	0												
Absolute position = 184'085 μ m	No Error	No Warning	Parity OK												

Table 5

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4. Relation between absolute value and incremental output

If incremental signals are used, they must be in proper relationship to the absolute values, to be properly processed by the subsequent electronics.

Correct relationship - see signal diagram:

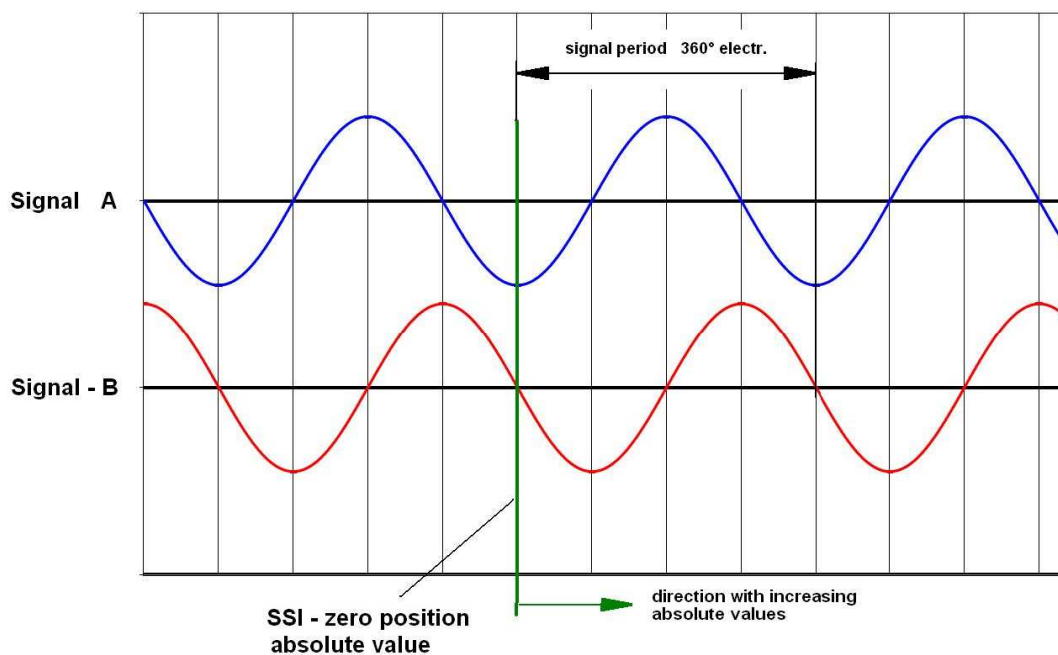


Diagram 4

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