System: **ABSYS - Absolute Encoders**
Based on the AMOSIN® – Inductive Measuring Principle

Types:

WMIA	Absolute Angular Encoder
LMIA	Absolute Linear Encoder

(for additional details, refer to www.amo-gmbh.com)

Implementation of output interface in ABSYS encoders:

SSI

Document History:

Revision	Date	Author	Notes:
00	12.03.2009	A. Pommer	Initial version
	06.10.2011	A. Pommer	Design of the document changed (front page).
01	03.11.2011	A. Pommer	Description for Error and Warning bits
02	11.11.2011	Paul Tutzu	SSI Frame definition improved (rotary and linear encoder)
03	25.06.2012	A. Pommer	Add configuration for LMKA-2x100 (scale length > 9200mm)
04	18.12.2013	A. Pommer	Add additional no. of databits. See Table 3
05	04.03.2014	A. Pommer	Add additional no. of databits. See Table 3 / new Order Codes
05.1	05.05.2014	A. Pommer	Changes in: Table 1 / Supply Voltage Power Consumption Table3 / min. clock frequency

1. Power supply Specification

Supply voltage:	DC 3,5V to 5,5V
Power consumption:	max. 250 mA@5,0V (360mA@3,5V / 230mA@5,5V)
Ripple on supply voltage:	max. 50mVpp

Table 1

2. Turn on Time

Turn on time reading head:	≤ 2 s

Table 2

3. Interface Protocol

3.1 General Description

The position value is transmitted synchronously to the clock signal of the control system starting with the most significant bit (MSB). When non-operational the clock as well as the data line is high. As soon as the clock signal of a clock sequence changes for the first time from high (H) to low (L), the parallel data will be stored in an internal shift register. This ensures that the data cannot change during the transmission of a position value. With the following rising edge transition of the clock signal, the transmission begins with the most significant bit (MSB). With each following rising edge transition of the clock signal, the next lower significant bit is set on the output of the data line. After the least significant bit was shifted out, the last rising edge transition of the clock signal switches the data line to low (transmission end).

> Description – Error bit:

The integrity of the absolute position is checked every 0.5mm. When an incorrect absolute position is read by the ABSYS encoder the **Error bit** is set to "1" (Error active). The error may occur after Power-On or during normal operation

> Description – Warning bit:

Warning bit is not used. Warning is always inactive and it is set to "0".

> End of transmission / pause time:

After the last falling edge of the clock signal, a retriggerable mono-flop determines with its internal delay time tm, how long it will take until the encoder can be selected for the next transmission. With this, the minimal admissible break time between two successive clock sequences is determined.

3.2 Timing

Clock frequency :	200 kHz – 1 MHz		
Monoflop time - t_m:	30µs		
Logic state during t_m:	Dataline – low (see diagram 1)		
Number of bits	**Order Code**	**Number of bits - m:**	**Number of databits - N:**
	WMKA-2x100.**1** WMKA-2x100.**2** LMKA-**1**x100.**1** LMKA-**1**x100.**2**	28	25
	LMKA-**2**x100.**1** LMKA-**2**x100.**2**	31	28
	WMKA-2x100.**4** WMKA-2x100.**5** LMKA-xx100.**4** LMKA-xx100.**5**	33	30
Number of special bits:	3		
Type of special bits:	S0 ... parity [even]		
	S1 ... warning		
	S2 ... error		
Placement of special bits	placed after data bits (see diagram 1)		
Logic state of special bits	high active		

Notes:
1) Scale length > 9200mm up to 32000mm
2) Recommended for new projects

Table 3

Timing diagram:

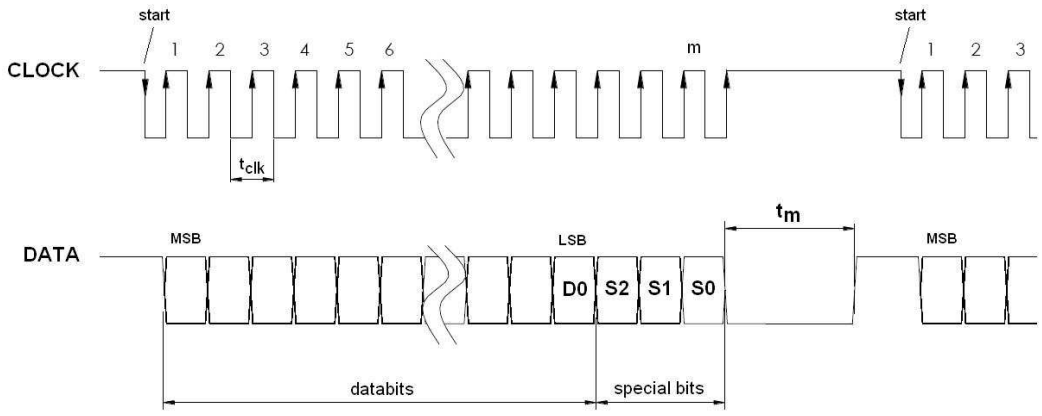

Diagram 1

3.3 Coding of absolute value

Position data is coded binary (for details - see table 4). First data bit represents MSB.

3.3.1 Absolute encoder rotary – WMIA

Absolute rotary coding:

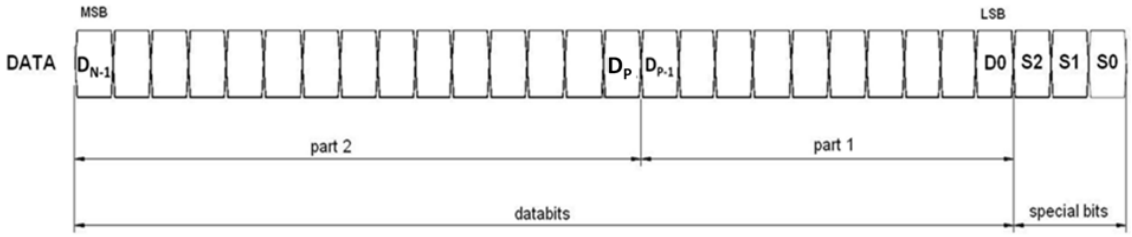

Diagram 2

Databits :	
part 2:	**$D_{N-1} \div D_P$** circumference in mm, binary coded
part 1:	**$D_{P-1} \div D_0$** position inside one grating pitch [1)]
	"P"-value depends on the ***Resolution in bit per grating pitch*** • When Resolution/Pitch is 10bit → P = 10 • When Resolution/Pitch is 12bit → P = 12
	Example: WMKA-20100.100-256-1,5-5 • *Resolution in bit per grating pitch* is 10 bits (N=25, P=10): - Data bits – Part 1 (10bits): **$D_9 \div D_0$** - Data bits – Part 2 (15bits): **$D_{24} \div D_{10}$** • SSI Frame:

Data Bits		Special Bits		
Part 2	**Part 1**	**Er**	**Wr**	**Par**
000000010110011	1100010101	0	0	0
179 (179/255)	789 (789/1023)	**No Error**	**No Warning**	**Parity OK**

Notes: [1)] grating pitch = 1mm

Table 4

3.3.1 Absolute encoder linear – LMIA

Absolute linear coding:

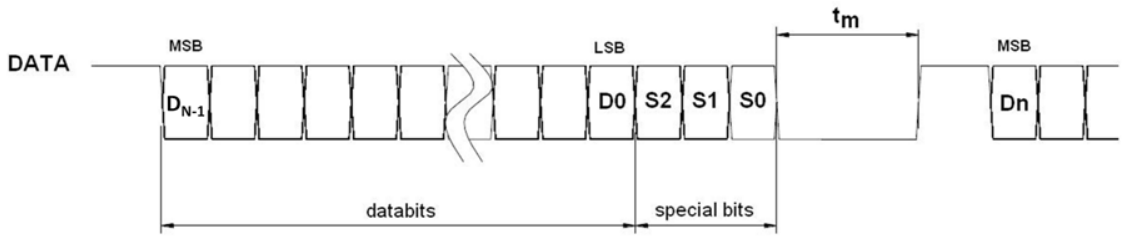

Diagram 3

Databits :	**$D_{N-1} \div D_0$** • 1 LSB represents the Encoder Resolution (e.g. 1µm) - binary coded. • Data is right aligned. Unused MSBs are filled with '0'.
	Example: LMKA-11100.100-1,5-5 • Resolution is 1µm • Data bits width: 25 bits (N = 25) • SSI Frame:

Data Bits	Special Bits		
	Er	Wr	Par
0000000101100111100010101	0	0	0
Absolute position = 184'085 µm	No Error	No Warning	Parity OK

Table 5

4. Relation between absolute value and incremental output

If incremental signals are used, they must be in proper relationship to the absolute values, to be properly processed by the subsequent electronics.

Correct relationship - see signal diagram:

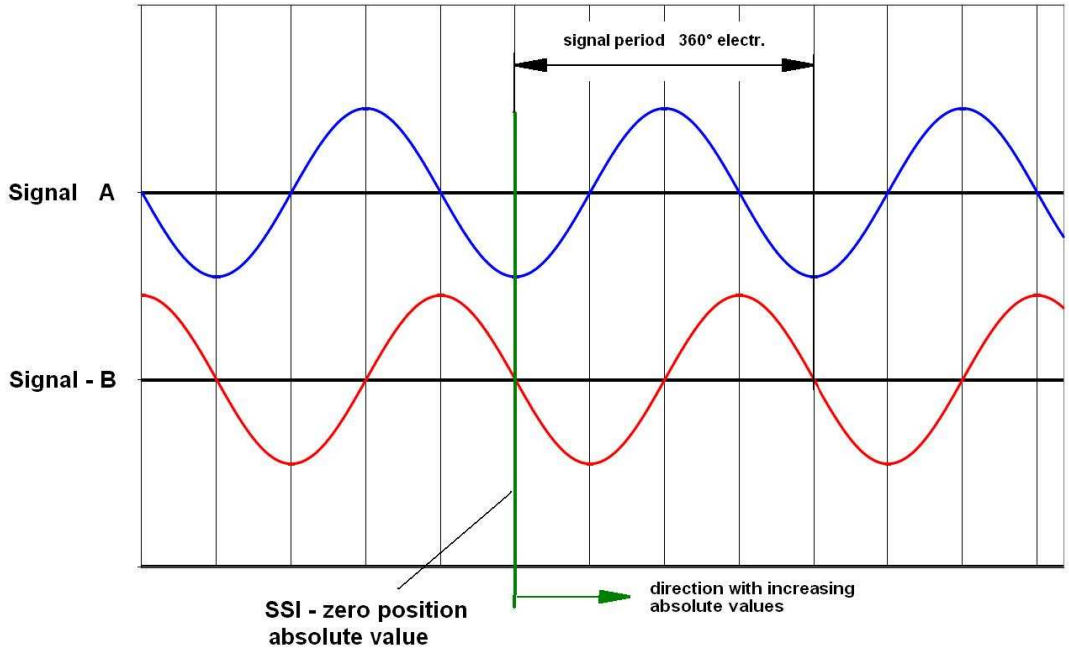

Diagram 4